IN THE CLAIMS

Please amend claim 68 as follows below.

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1. (Original) A method of processing for a semiconductor device, the method comprising:

providing a wafer including a substrate;

forming a plurality of sidewalls around a plurality of cylindrical pedestals above a surface of the substrate;

removing the plurality of cylindrical pedestals; and

vertically etching horizontal surfaces of a first material located around the plurality of sidewalls.

2. (Original) The method of claim 1, wherein,

the plurality of sidewalls provide an etch stop.

3. (Original) The method of claim 2, wherein,

the plurality of sidewalls protect the first material under the plurality of sidewalls from being etched during the vertical etching of the first material.

4. (Original) The method of claim 1, further comprising:

removing the plurality of sidewalls.

5. (Original) The method of claim 1, further comprising:

diffusing a dopant into the first material located around the plurality of sidewalls.

6. (Original) The method of claim 1, further comprising:

diffusing a dopant into a second material around the plurality of sidewalls.

7. (Original) The method of claim 1, further comprising:

diffusing a dopant into the first material and a second material around the plurality of sidewalls.

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8. (Original) The method of claim 1, further comprising:

diffusing a dopant into the first material or a second material around the plurality of sidewalls.

9. (Original) The method of claim 8, wherein,

the plurality of sidewalls provide an etch stop and a diffusion barrier.

10. (Original) The method of claim 9, wherein,

the plurality of sidewalls protect the first material under the plurality of sidewalls from receiving a dopant during the diffusing of the dopant into the first material or the second material.

11. (Original) The method of claim 9, wherein,

the plurality of sidewalls protect the second material under the plurality of sidewalls from receiving a dopant during the diffusing of the dopant into the first material and the second material.

12. (Original) The method of claim 9, wherein,

the plurality of sidewalls protect the first material and the second material under the plurality of sidewalls from receiving a dopant during the diffusing of the dopant into the first material or the second material.

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13. (Original) A method of processing for a semiconductor device, the method comprising:

providing a wafer including a substrate;

forming a plurality of sidewalls around a plurality of cylindrical pedestals above a surface of the substrate;

removing the plurality of cylindrical pedestals; and

diffusing a dopant into a first material located around the plurality of sidewalls.

14. (Original) The method of claim 13, wherein,

the plurality of sidewalls provide a diffusion barrier.

15. (Original) The method of claim 14, wherein,

the plurality of sidewalls protect the first material under the plurality of sidewalls from receiving a dopant during the diffusing of the dopant into the first material.

16. (Original) The method of claim 13, further comprising:

removing the plurality of sidewalls.

17. (Original) The method of claim 13, further comprising:

vertically etching horizontal surfaces of the first material located around the plurality of sidewalls.

18. (Original) The method of claim 13, further comprising:

vertically etching horizontal surfaces of a second material located around the plurality of sidewalls.

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19. (Original) The method of claim 13, further comprising:

vertically etching horizontal surfaces of the first material and a second material located around the plurality of sidewalls.

20. (Original) The method of claim 13, further comprising:

vertically etching horizontal surfaces of the substrate located around the plurality of sidewalls.

21. (Original) The method of claim 13, further comprising:

vertically etching horizontal surfaces of the first material or a second material located around the plurality of sidewalls.

22. (Original) The method of claim 21, wherein,

the plurality of sidewalls provide a diffusion barrier and an etch stop.

23. (Original) The method of claim 22, wherein,

the plurality of sidewalls protect the first material under the plurality of sidewalls from being etched during the etching of the first material.

24. (Original) The method of claim 22, wherein,

the plurality of sidewalls protect the second material under the plurality of sidewalls from being etched during the etching of the second material.

25. (Original) The method of claim 22, wherein,

the plurality of sidewalls protect the first material and the second material under the plurality of sidewalls from being etched during the vertical etching of the first material and the second material.

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26. (Original) The method of claim 22, wherein,

the plurality of sidewalls protect the first material or the second material under the plurality of sidewalls from being etched during the vertical etching of the first material or the second material.

27. (Original) A method of processing for a semiconductor device, the method comprising:

providing a substrate of the semiconductor device;

forming a plurality of sidewalls above a surface of the substrate;

vertically etching horizontal surfaces of a material located around the plurality of sidewalls; and

diffusing a dopant around the plurality of sidewalls.

28. (Original) The method of claim 27, wherein,

the plurality of sidewalls are formed by

forming a plurality of cylindrical pedestals above a surface of the substrate,

depositing a sidewall material layer over the cylindrical pedestals and the substrate,

vertically etching the horizontal surfaces of the sidewall material, and

etching away the plurality of cylindrical pedestals.

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29. (Original) The method of claim 27, wherein,

the vertical etching of horizontal surfaces of the material located around the plurality of sidewalls is performed using a substantially anisotropic etchant.

30. (Original) The method of claim 27, wherein,

the plurality of sidewalls provide an etch stop and a diffusion barrier.

31. (Original) The method of claim 30, wherein,

the plurality of sidewalls protect the material under the plurality of sidewalls from being etched during the etching of the material around the plurality of sidewalls and the plurality of sidewalls protect the material under the plurality of sidewalls from receiving the dopant during the diffusing of the dopant around the plurality of sidewalls.

32. (Original) A method of processing for a semiconductor device, the method comprising:

providing a substrate of the semiconductor device;

forming a plurality of sidewalls above a surface of the substrate; and

diffusing a dopant around the plurality of sidewalls.

33. (Original) The method of claim 32, wherein,
the plurality of sidewalls provide a diffusion barrier.

34. (Original) The method of claim 32, wherein,
the plurality of sidewalls are formed by
forming a plurality of cylindrical pedestals above a surface of the substrate,
depositing a sidewall material layer over the cylindrical pedestals and the substrate,
vertically etching the horizontal surfaces of the sidewall material, and
etching away the plurality of cylindrical pedestals.

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35. (Original) The method of claim 32, further comprising:
vertically etching horizontal surfaces of a material located around the plurality of sidewalls.

36. (Original) The method of claim 35, wherein,
the plurality of sidewalls provide an etch stop and a diffusion barrier.

37. (Original) The method of claim 35, wherein,
the vertical etching of horizontal surfaces of the material located around the plurality of sidewalls is performed using a substantially anisotropic etchant.

38. (Original) The method of claim 36, wherein,

the plurality of sidewalls protect the material under the plurality of sidewalls from being etched during the vertical etching of horizontal surfaces of the material around the plurality of sidewalls and the plurality of sidewalls protect the material under the plurality of sidewalls from receiving the dopant during the diffusing of the dopant around the plurality of sidewalls.

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39. (Original) The method of claim 35, wherein,

the material located around the plurality of sidewalls which is vertically etched is the substrate.

40. (Original) The method of claim 35, wherein,

the material located around the plurality of sidewalls which is vertically etched is a layer exposed over a surface of the substrate and protected under the plurality of sidewalls.

41. (Original) A method of processing for a semiconductor device, the method comprising:

providing a substrate of the semiconductor device;

forming a plurality of sidewalls above a surface of the substrate; and

vertically etching horizontal surfaces of a material located around the plurality of sidewalls.

42. (Original) The method of claim 41, wherein,

the plurality of sidewalls provide an etch stop.

43. (Original) The method of claim 41, wherein,

the material located around the plurality of sidewalls which is horizontally etched is the substrate.

44. (Original) The method of claim 41, wherein,

the material located around the plurality of sidewalls which is horizontally etched is an epitaxial layer of the substrate.

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45. (Original) The method of claim 41, wherein,

the material located around the plurality of sidewalls which is horizontally etched is a layer exposed over a surface of the substrate and protected under the plurality of sidewalls.

46. (Original) The method of claim 41, wherein,

the vertical etching of horizontal surfaces of the material located around the plurality of sidewalls is performed using a substantially anisotropic etchant.

47. (Original) The method of claim 41, wherein,

the plurality of sidewalls are formed by

forming a plurality of cylindrical pedestals above a surface of the substrate,

depositing a sidewall material layer over the cylindrical pedestals and the substrate,

vertically etching the horizontal surfaces of the sidewall material, and

etching away the plurality of cylindrical pedestals.

48. (Original) The method of claim 41, further comprising:

diffusing a dopant around the plurality of sidewalls.

49. (Original) The method of claim 48, wherein,
the plurality of sidewalls provide an etch stop and a diffusion barrier.

50. (Original) The method of claim 49, wherein,
the plurality of sidewalls protect the material under the plurality of sidewalls from being etched during the vertical etching of the material located around the plurality of sidewalls and the plurality of sidewalls protect the material under the plurality of sidewalls from receiving the dopant during the diffusing of the dopant around the plurality of sidewalls.

51. (Original) The method of claim 48, wherein,
the dopant is diffused into the substrate around the plurality of sidewalls.

52. (Original) The method of claim 48, wherein,
the dopant is diffused into the material around the plurality of sidewalls.

53-57. (Cancelled)

58. (Original) A system for manufacturing a semiconductor device comprising:
a container for receiving a semiconductor wafer;
the semiconductor wafer having a plurality of sidewalls formed over a substrate;
a means for etching a material around the plurality of sidewalls; and
wherein the plurality of sidewalls provide an etch stop to protect the material underneath the plurality of sidewalls from being etched.

59. (Original) The system of claim 58, wherein,
the means for etching the material is a gas, plasma, or liquid.

60. (Original) The system of claim 58, wherein,
the means for etching includes an excitation field to excite ions in a gas, plasma, or liquid.

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61. (Original) The system of claim 58, further comprising:
a means for diffusing dopants into a material around the plurality of sidewalls; and
wherein the plurality of sidewalls provide a diffusion barrier to protect the material underneath the plurality of sidewalls from being implanted.

62. (Original) The system of claim 61, wherein,
the means for diffusing dopants in the material is a gas, plasma, or liquid.

63. (Original) The system of claim 58, wherein,
the container is a chamber, an oven, or a bath tub.

64. (Original) A system for manufacturing a semiconductor device comprising:
a container for receiving a semiconductor wafer;
the semiconductor wafer having a plurality of sidewalls formed over a substrate;
a means for diffusing a dopant into a material around the plurality of sidewalls; and
wherein the plurality of sidewalls provide a diffusion barrier to protect the material underneath the plurality of sidewalls from being implanted.

65. (Original) The system of claim 64, wherein,

the means for diffusing dopants into the material is a gas, plasma, or liquid.

66. (Original) The system of claim 64, wherein,

the means for diffusing includes an excitation field to implant the dopant into the material around the plurality of sidewalls.

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67. (Original) The system of claim 64, wherein,

the means for diffusing includes a source of heat to diffuse the dopant into the material around the plurality of sidewalls.

68. (Currently Amended) The system of claim ~~64~~ 67, wherein,

the source of heat is an oven.

69. (Original) The system of claim 64, further comprising:

a means for etching into a material around the plurality of sidewalls; and

wherein the plurality of sidewalls provide an etch stop to protect the material underneath the plurality of sidewalls from being etched.

70. (Original) The system of claim 69, wherein,

the means for etching the material is a gas, plasma, or liquid.

71. (Original) The system of claim 70, wherein,

the means for etching includes an excitation field to excite ions in a gas, plasma, or liquid.

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72. (Original) The system of claim 71, wherein,

the container is a chamber, an oven, or a bath tub.